

Notice of References Cited	Application/Control No. 09/836,480	Applicant(s)/Patent Under Reexamination MIYANO, KAZUTAKA	
	Examiner Ted M Wang	Art Unit 2634	Page 1 of 1

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	C	US-4,438,353	03-1984	Sano et al.	326/100
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	L	US-			
	M	US-			

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NON-PATENT DOCUMENTS

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	U	Low-jitter process-independent DLL and PLL based on self-biased techniques, Maneatis, J.G.; Solid-State Circuits, IEEE Journal of, Volume: 31, Issue: 11, Nov. 1996, Pages:1723 – 1732
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.